

## General Description

The MAX14980 quad-channel redriver is designed to redrive two full lanes of SAS or SATA signals up to 6.0GT/s (gigatransfers per second) and operates from a single +3.3V supply.

The MAX14980 features independent input equalization and output preemphasis. It enhances signal integrity at the receiver by equalizing the signal at the input and establishing preemphasis at the output of the device. SAS and SATA OOB (out-of-band) signaling is supported using high-speed amplitude detection on the inputs and squelch on the corresponding outputs. Inputs and outputs are all internally 50Ω terminated and must be AC-coupled to the SAS/SATA controller IC and SAS/SATA device.

The MAX14980 is available in a small 42-pin, 3.5mm x 9mm, TQFN package with flow-through traces for ease of layout. This device is specified over the -40°C to +85°C extended operating temperature range.

## Applications

- Industrial/Embedded PCs
- Computer on Modules
- Carrier Boards
- Test Equipment
- Rack Server Industrial PCs
- Medical Equipment

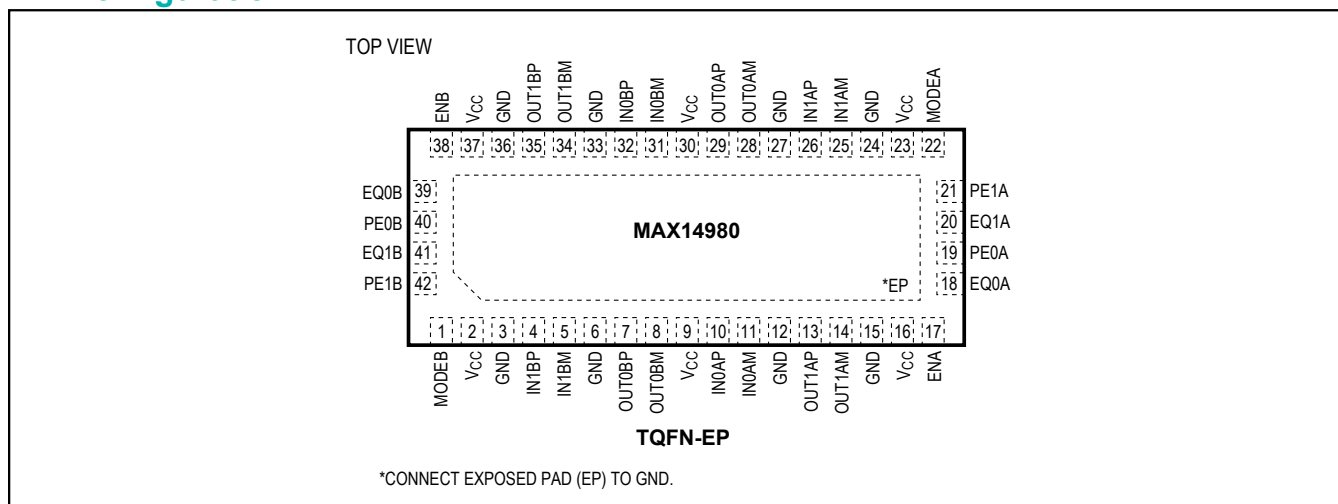
## Benefits and Features

- High Performance Solution Designed to Overcome Lossy Channels
  - 3dB of Independent (per Channel) Selectable Input EQ and Output Preemphasis
  - Compensates up to 30in of Channel Losses with Deterministic Jitter: 23ps<sub>P-P</sub> (max); Random Jitter: 1.8ps<sub>RMS</sub> (max)
  - 8dB (typ) of Return Loss Up to 3.0GHz
- Designed to Reliably Operate in Harsh Environments
  - Industrial Temperature Rated: -40°C to +85°C
  - ±2.5kV Human Body Model (HBM) ESD Protection on All Pins
  - Housed in a Flow-Through (42-Pin, 3.5mm x 9.0mm) TQFN Package or Resistance to Vibration/Shocks
- Ease of Design and Layout
  - Single 3.3V Operation
  - Internal Input/Output 50Ω Termination Resistors

**Ordering Information** appears at end of data sheet.

For related parts and recommended products to use with this part, refer to [www.maximintegrated.com/MAX14980.related](http://www.maximintegrated.com/MAX14980.related).

## Pin Configuration



## Absolute Maximum Ratings

(Voltages referenced to GND.)

|                                                                          |                              |
|--------------------------------------------------------------------------|------------------------------|
| $V_{CC}$ .....                                                           | -0.3V to +4.0V               |
| All Other Pins .....                                                     | -0.3V to ( $V_{CC} + 0.3V$ ) |
| Continuous Current ( $PE_{-}$ , $EQ_{-}$ , $MODE_{-}$ ).....             | $\pm 15mA$                   |
| Peak Current (for 10kHz, 1% duty cycle)<br>( $IN_{-}$ , $OUT_{-}$ )..... | $\pm 100mA$                  |

Continuous Power Dissipation ( $T_A = +70^{\circ}C$ )

|                                                              |                                   |
|--------------------------------------------------------------|-----------------------------------|
| TQFN (derate 35.7mW/ $^{\circ}C$ above $+70^{\circ}C$ )..... | 2857mW                            |
| Operating Temperature Range.....                             | $-40^{\circ}C$ to $+85^{\circ}C$  |
| Storage Temperature Range .....                              | $-55^{\circ}C$ to $+150^{\circ}C$ |
| Junction Temperature.....                                    | $+150^{\circ}C$                   |
| Lead Temperature (soldering, 10s) .....                      | $+300^{\circ}C$                   |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Package Thermal Characteristics (Note 1)

TQFN

Junction-to-Case Thermal Resistance ( $\theta_{JC}$ ) .....  $2^{\circ}C/W$       Junction-to-Ambient Thermal Resistance ( $\theta_{JA}$ ) .....  $28^{\circ}C/W$

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

## Electrical Characteristics

( $V_{CC} = +3.0V$  to  $+3.6V$ ,  $C_{COUPLE} = 12nF$ ,  $R_L = 50\Omega$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $V_{CC} = +3.3V$ ,  $T_A = +25^{\circ}C$ .) (Note 2)

| PARAMETER                                   | SYMBOL         | CONDITIONS                                     | MIN  | TYP | MAX  | UNITS             |
|---------------------------------------------|----------------|------------------------------------------------|------|-----|------|-------------------|
| Operating Power-Supply Range                | $V_{CC}$       |                                                | 3.0  |     | 3.6  | V                 |
| Operating Supply Current                    | $I_{CC}$       | $EQ_{-} = PE_{-} = GND$                        |      | 280 | 350  | mA                |
|                                             |                | $EQ_{-} = PE_{-} = V_{CC}$                     |      | 350 | 440  |                   |
| Standby Supply Current                      | $I_{STBY}$     | $EN_{-} = GND$                                 |      | 32  | 40   | mA                |
| Input Termination                           | $R_{RX-SE}$    | Single-ended to $V_{CC}$                       | 42.5 |     | 57.5 | $\Omega$          |
| Output Termination                          | $R_{TX-SE}$    | Single-ended to $V_{CC}$                       | 42.5 |     | 57.5 | $\Omega$          |
| <b>AC PERFORMANCE</b>                       |                |                                                |      |     |      |                   |
| Differential Input Return Loss<br>(Note 3)  | $S_{DD11}$     | $0.1GHz \leq f \leq 0.3GHz$                    | -10  |     |      | dB                |
|                                             |                | $0.3GHz \leq f \leq 3.0GHz$                    | -7.9 |     |      |                   |
|                                             |                | $3.0GHz \leq f \leq 6.0GHz$                    | 0    |     |      |                   |
| Common-Mode Input Return Loss<br>(Note 3)   | $S_{CC11}$     | $0.1GHz \leq f \leq 0.3GHz$                    | -6   |     |      | dB                |
|                                             |                | $0.3GHz \leq f \leq 3.0GHz$                    | -5   |     |      |                   |
|                                             |                | $3.0GHz \leq f \leq 6.0GHz$                    | 0    |     |      |                   |
| Differential Output Return Loss<br>(Note 3) | $S_{DD22}$     | $0.1GHz \leq f \leq 0.3GHz$                    | -10  |     |      | dB                |
|                                             |                | $0.3GHz \leq f \leq 3.0GHz$                    | -7.9 |     |      |                   |
|                                             |                | $3.0GHz \leq f \leq 6.0GHz$                    | 0    |     |      |                   |
| Common-Mode Output Return Loss<br>(Note 3)  | $S_{CC22}$     | $0.1GHz \leq f \leq 0.3GHz$                    | -6   |     |      | dB                |
|                                             |                | $0.3GHz \leq f \leq 3.0GHz$                    | -4   |     |      |                   |
|                                             |                | $3.0GHz \leq f \leq 6.0GHz$                    | 0    |     |      |                   |
| Differential Input Voltage                  | $V_{IN-DIFF}$  | SAS 1.5, 3.0, or 6.0GT/s, $MODE_{-} = GND$     | 275  |     | 1600 | mV <sub>P-P</sub> |
|                                             |                | SATA 1.5, 3.0, or 6.0GT/s, $MODE_{-} = V_{CC}$ | 225  |     | 1600 |                   |
| Input Equalization                          | EQ             | $EQ_{-} = V_{CC}$ (Note 4)                     |      | 3   |      | dB                |
| Differential Output Voltage                 | $V_{OUT-DIFF}$ | $f = 750MHz$ , $PE_{-} = GND$                  | 750  |     | 1200 | mV <sub>P-P</sub> |
| Output Preemphasis                          | PE             | $PE_{-} = V_{CC}$ , Figure 1                   |      | 3   |      | dB                |

**Electrical Characteristics (continued)**

( $V_{CC} = +3.0V$  to  $+3.6V$ ,  $C_{COUPLE} = 12nF$ ,  $R_L = 50\Omega$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise noted. Typical values are at  $V_{CC} = +3.3V$ ,  $T_A = +25^\circ C$ .) (Note 2)

| PARAMETER                          | SYMBOL                | CONDITIONS                                                        | MIN | TYP | MAX | UNITS             |
|------------------------------------|-----------------------|-------------------------------------------------------------------|-----|-----|-----|-------------------|
| Propagation Delay                  | $t_{PD}$              | $PE\_ = EQ\_ = GND$                                               |     | 300 |     | ps                |
| Output Transition Time             | $T_{TX-RF}$           | $PE\_ = GND$ , 20% to 80%                                         | 30  |     |     | ps                |
| Differential Output Skew Same Pair | $T_{SK}$              |                                                                   |     | 10  |     | ps                |
| Deterministic Jitter               | $T_{DJ}$              | K28.5 pattern, 6.0GT/s, $PE\_ = EQ\_ = GND$ (Note 3)              |     |     | 23  | ps <sub>P-P</sub> |
| Random Jitter                      | $T_{RJ}$              | D10.2 pattern, 6.0GT/s, $PE\_ = EQ\_ = GND$                       |     |     | 1.8 | ps <sub>RMS</sub> |
| OOB Squelch Threshold              | $V_{SQ-DIFF}$         | MODE_ = GND, $f = 0.75GHz$                                        | 120 |     | 220 | mV <sub>P-P</sub> |
|                                    |                       | MODE_ = $V_{CC}$ , $f = 0.75GHz$                                  | 75  |     | 200 |                   |
| OOB Squelch Entry Time             | $T_{OOB,SQ}$          | $f = 0.75GHz$ (Note 3)                                            |     |     | 5   | ns                |
| OOB Exit Time                      | $T_{OOB,EX}$          | $f = 0.75GHz$ (Note 3)                                            |     |     | 9   | ns                |
| OOB Differential Offset Delta      | $\Delta V_{OOB,DIFF}$ | Difference between OOB and active-mode output offset              | -50 |     | +50 | mV                |
| OOB Common-Mode Offset Delta       | $\Delta V_{OOB,CM}$   | Difference between OOB and active-mode output common-mode voltage | -30 |     | +30 | mV                |
| OOB Output Disable                 | $V_{OOB,OUT}$         | OOB disabled output level                                         |     |     | 30  | mV <sub>P-P</sub> |
| <b>CONTROL LOGIC INPUTS</b>        |                       |                                                                   |     |     |     |                   |
| Input Logic-High                   | $V_{IH}$              |                                                                   | 1.4 |     |     | V                 |
| Input Logic-Low                    | $V_{IL}$              |                                                                   |     |     | 0.6 | V                 |
| Input Logic Hysteresis             | $V_{HYST}$            |                                                                   |     | 75  |     | mV                |
| Input Leakage Current              | $I_{IN}$              | $V_{CC} = 3.3V$ , $V_{IN} = 0.5V$ or $1.5V$                       | -50 |     | +50 | $\mu A$           |

**Note 2:** All devices are 100% production tested at  $T_A = +85^\circ C$ . All temperature limits are guaranteed by design.

**Note 3:** Guaranteed by design.

**Note 4:** EQ (input equalization) as employed in this device refers to the equivalent of adding preemphasis before the input. For example, input EQ of 3dB would show the same waveform as output PE of 3dB (see Figure 1).

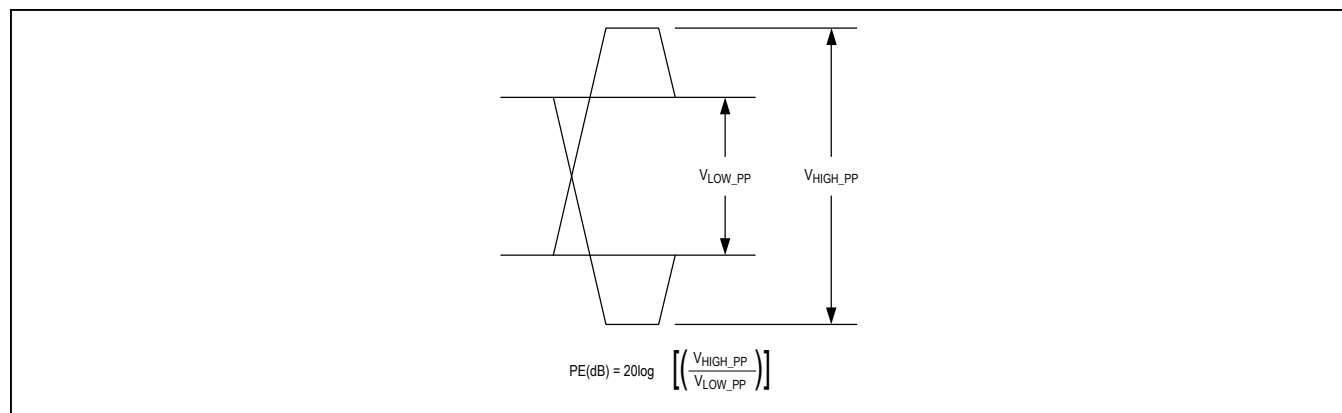
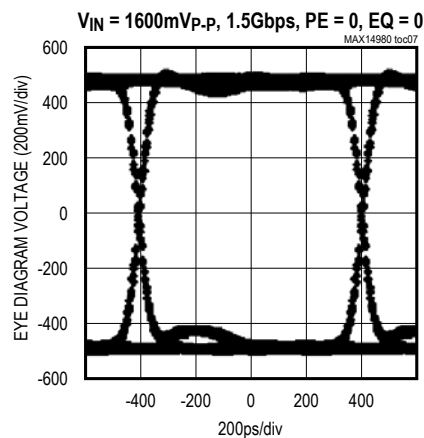
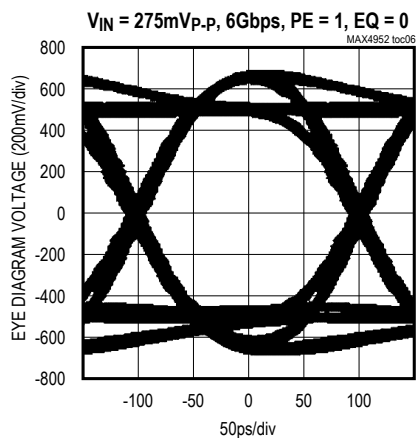
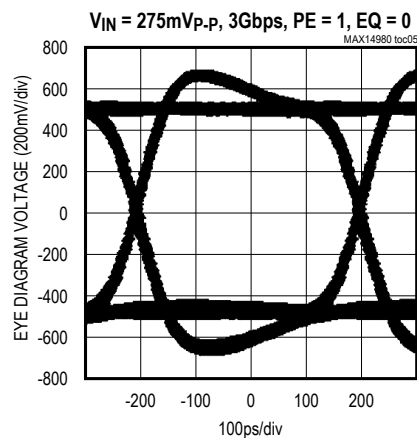
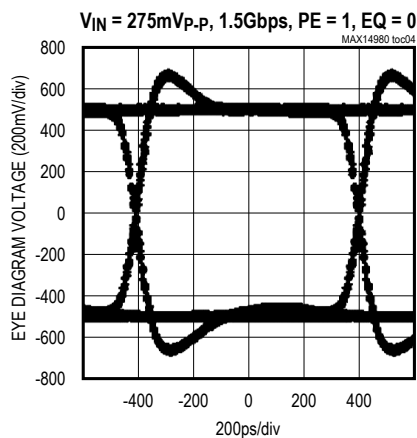
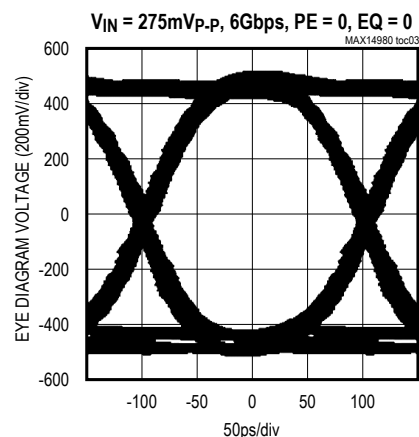
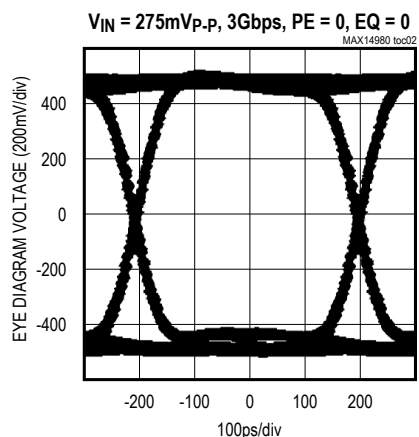
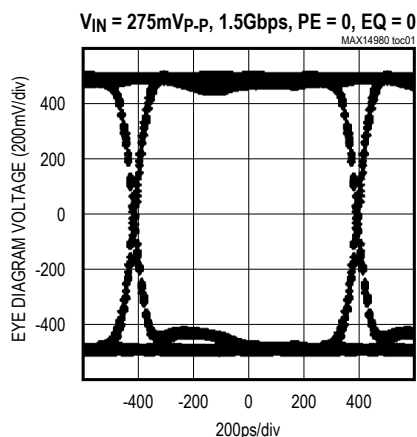
**Timing Diagram**

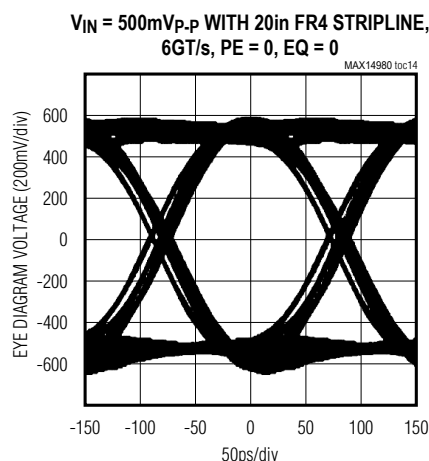
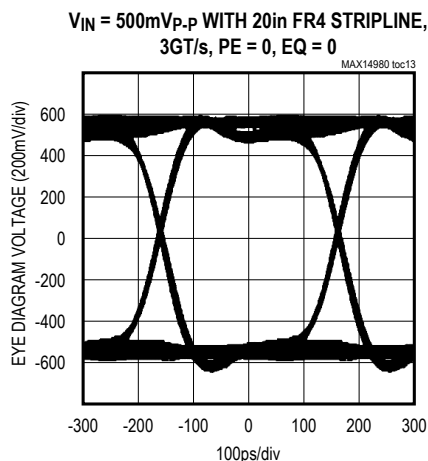
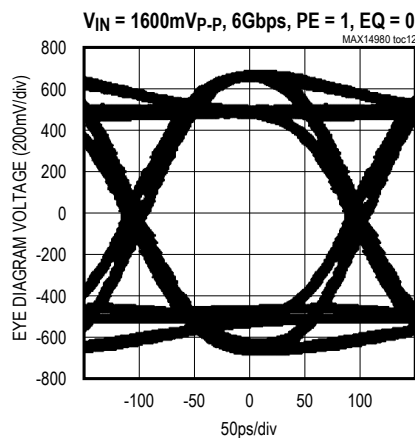
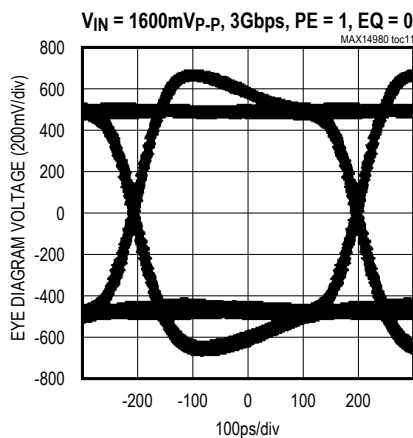
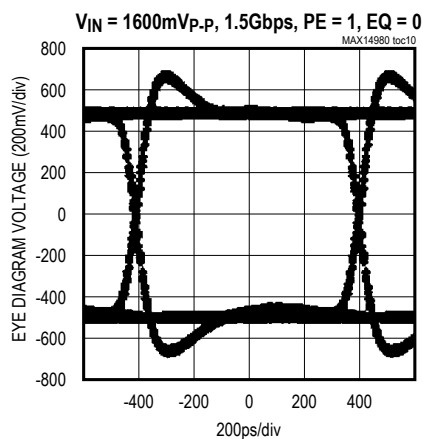
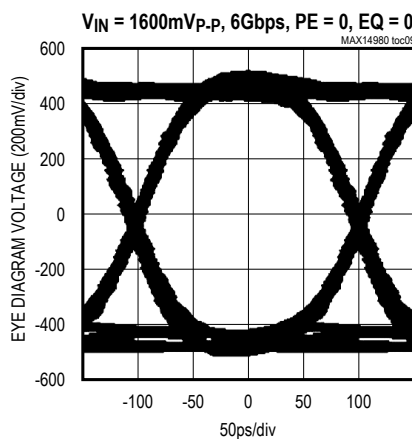
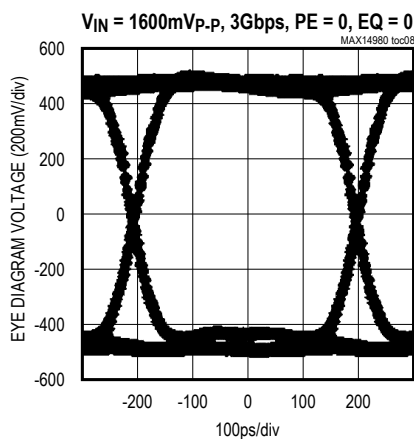
Figure 1. Output Preemphasis

### Typical Operating Characteristics

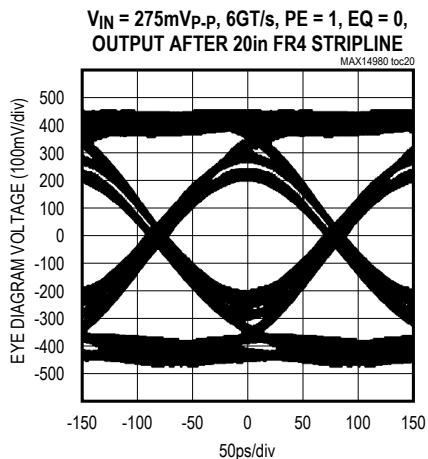
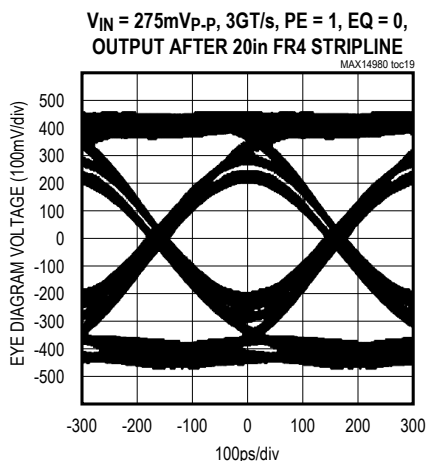
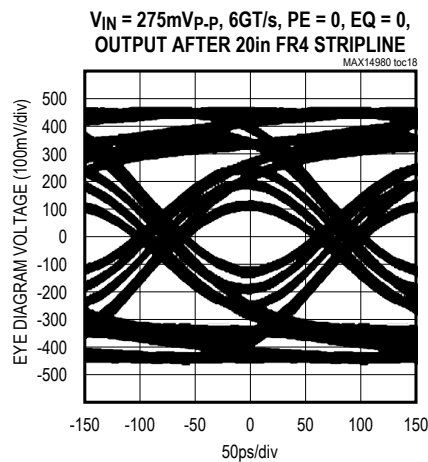
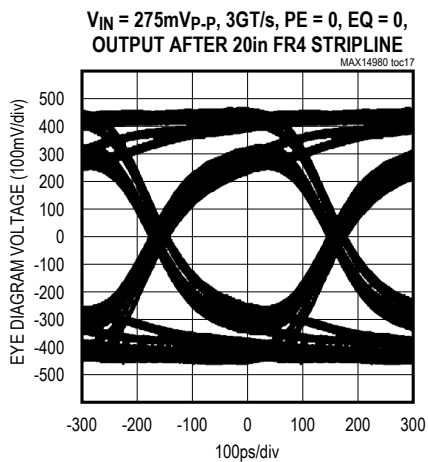
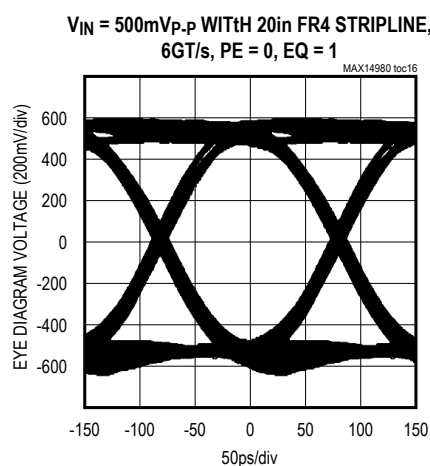
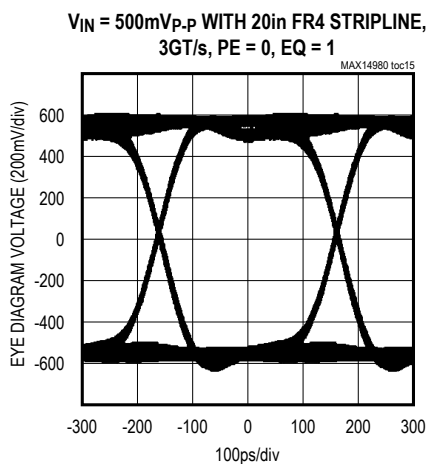
( $V_{CC} = +3.3V$ ,  $T_A = +25^\circ C$ , all eye diagrams measured using K28.5 pattern.)



## Typical Operating Characteristics (continued)

(V<sub>CC</sub> = +3.3V, T<sub>A</sub> = +25°C, all eye diagrams measured using K28.5 pattern.)

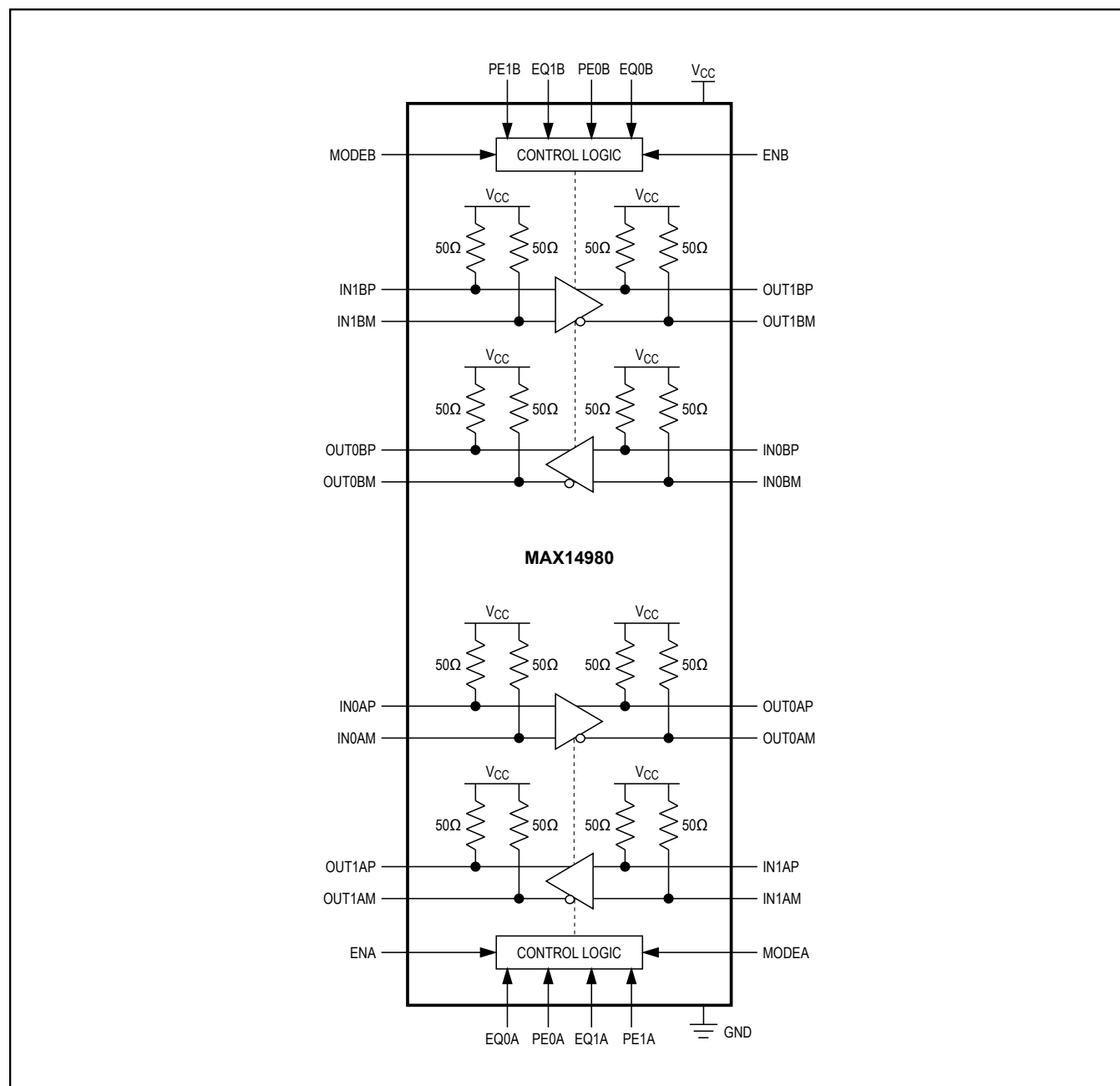
## Typical Operating Characteristics (continued)

(V<sub>CC</sub> = +3.3V, T<sub>A</sub> = +25°C, all eye diagrams measured using K28.5 pattern.)

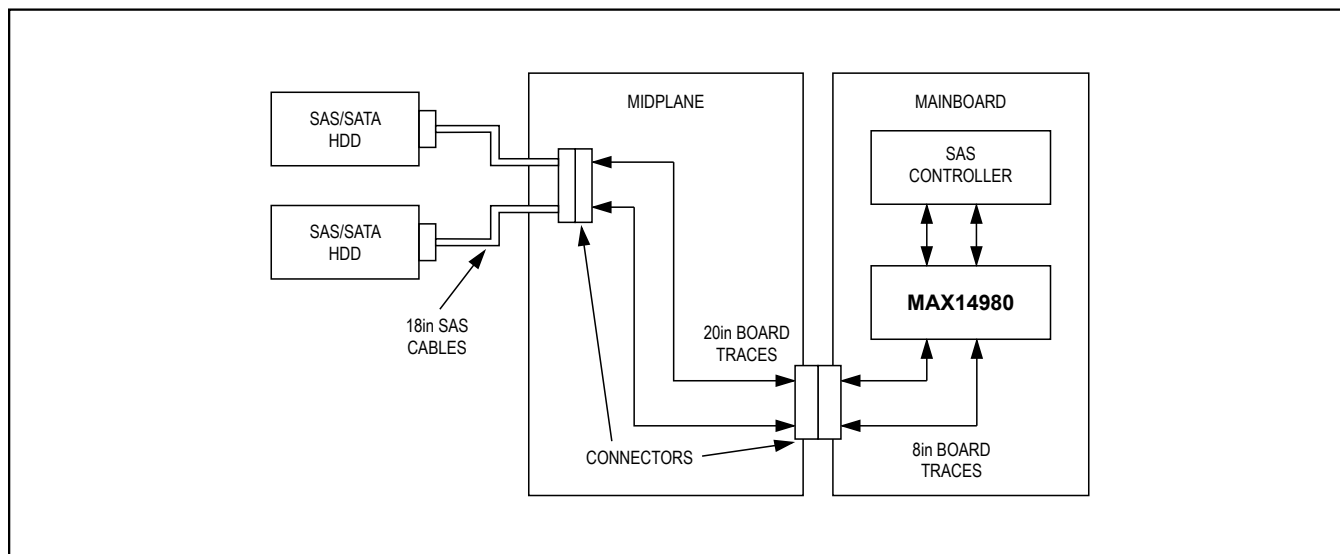
## Pin Description

| PIN                          | NAME            | FUNCTION                                                                                                                                                                                |
|------------------------------|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1                            | MODEB           | OOB Threshold Logic Input B. MODEB is internally pulled down.                                                                                                                           |
| 2, 9, 16, 23, 30, 37         | V <sub>CC</sub> | Positive Supply Voltage Input. Bypass V <sub>CC</sub> to GND with 2.2μF and 0.01μF capacitors in parallel as close as possible to the device, recommended on each V <sub>CC</sub> pin.  |
| 3, 6, 12, 15, 24, 27, 33, 36 | GND             | Ground                                                                                                                                                                                  |
| 4                            | IN1BP           | Noninverting Input 1B                                                                                                                                                                   |
| 5                            | IN1BM           | Inverting Input 1B                                                                                                                                                                      |
| 7                            | OUT0BP          | Noninverting Output 0B                                                                                                                                                                  |
| 8                            | OUT0BM          | Inverting Output 0B                                                                                                                                                                     |
| 10                           | IN0AP           | Noninverting Input 0A                                                                                                                                                                   |
| 11                           | IN0AM           | Inverting Input 0A                                                                                                                                                                      |
| 13                           | OUT1AP          | Noninverting Output 1A                                                                                                                                                                  |
| 14                           | OUT1AM          | Inverting Output 1A                                                                                                                                                                     |
| 17                           | ENA             | Active-High Enable Input A. Drive ENA low to put A channels in standby mode. Drive ENA high to put A channels in normal operation. ENA is internally pulled down.                       |
| 18                           | EQ0A            | Channel 0A Input Equalizer Logic Input. EQ0A is internally pulled down.                                                                                                                 |
| 19                           | PE0A            | Channel 0A Output Preemphasis Logic Input. PE0A is internally pulled down.                                                                                                              |
| 20                           | EQ1A            | Channel 1A Input Equalizer Logic Input. EQ1A is internally pulled down.                                                                                                                 |
| 21                           | PE1A            | Channel 1A Output Preemphasis Logic Input. PE1A is internally pulled down.                                                                                                              |
| 22                           | MODEA           | OOB Threshold Logic Input A. MODEA is internally pulled down.                                                                                                                           |
| 25                           | IN1AM           | Inverting Input 1A                                                                                                                                                                      |
| 26                           | IN1AP           | Noninverting Input 1A                                                                                                                                                                   |
| 28                           | OUT0AM          | Inverting Output 0A                                                                                                                                                                     |
| 29                           | OUT0AP          | Noninverting Output 0A                                                                                                                                                                  |
| 31                           | IN0BM           | Inverting Input 0B                                                                                                                                                                      |
| 32                           | IN0BP           | Noninverting Input 0B                                                                                                                                                                   |
| 34                           | OUT1BM          | Inverting Output 1B                                                                                                                                                                     |
| 35                           | OUT1BP          | Noninverting Output 1B                                                                                                                                                                  |
| 38                           | ENB             | Active-High Enable Input B. Drive ENB low to put B channels in standby mode. Drive ENB high to put B channels in normal operation. ENB is internally pulled down.                       |
| 39                           | EQ0B            | Channel 0B Input Equalizer Logic Input. EQ0B is internally pulled down.                                                                                                                 |
| 40                           | PE0B            | Channel 0B Output Preemphasis Logic Input. PE0B is internally pulled down.                                                                                                              |
| 41                           | EQ1B            | Channel 1B Input Equalizer Logic Input. EQ1B is internally pulled down.                                                                                                                 |
| 42                           | PE1B            | Channel 1B Output Preemphasis Logic Input. PE1B is internally pulled down.                                                                                                              |
| —                            | EP              | Exposed Pad. Internally connected to GND. EP must be electrically connected to a ground plane for proper thermal and electrical operation. Do not use EP as the sole ground connection. |

## Functional Diagram



## Typical Application Circuit



## Detailed Description

The MAX14980 consists of four identical redrivers with input equalization and output preemphasis useful for SAS or SATA signals up to 6.0GT/s.

### Input/Output Terminations

Inputs and outputs are internally 50Ω terminated to  $V_{CC}$  (see the *Functional Diagram*) and must be AC-coupled using 12nF (max) capacitors to the SAS/SATA controller IC and SAS/SATA device for proper operation.

### Enable Inputs (ENA, ENB)

The MAX14980 features two active-high enable inputs (ENA, ENB). ENA and ENB have internal pulldown resistors of 70kΩ (typ). When ENA or ENB is driven low or left unconnected, the A or B channels enter low-power standby mode and the redrivers are disabled.

Drive ENA or ENB high to place channel A or B in normal operation (see Table 1).

### Out-of-Band Threshold Selector (MODEA, MODEB)

The MAX14980 provides full OOB signal support through high-speed amplitude detection circuitry. OOB differential input signals less than the internal OOB threshold ( $V_{SQ-DIFF}$ ) are detected as off and not passed to the output. This prevents the system from responding to unwanted noise. OOB differential input signals higher than  $V_{SQ-DIFF}$  are detected as on and passed to the output, allowing OOB signals to transmit through the MAX14980. The logic level of the MODE inputs sets  $V_{SQ-DIFF}$  for either SAS or SATA OOB signals (see Table 2). MODEA and MODEB have internal pulldown resistors of 70kΩ (typ).

**Table 1. Enable Inputs (ENA, ENB)**

| ENA | ENB | CHANNEL 1A | CHANNEL 0A | CHANNEL 1B | CHANNEL 0B |
|-----|-----|------------|------------|------------|------------|
| 0   | 0   | STANDBY    | STANDBY    | STANDBY    | STANDBY    |
| 0   | 1   | STANDBY    | STANDBY    | ENABLED    | ENABLED    |
| 1   | 0   | ENABLED    | ENABLED    | STANDBY    | STANDBY    |
| 1   | 1   | ENABLED    | ENABLED    | ENABLED    | ENABLED    |

**Table 2. Out-of-Band Logic Threshold (MODEA, MODEB)**

| MODEA | MODEB | CHANNEL 1A | CHANNEL 0A | CHANNEL 1B | CHANNEL 0B |
|-------|-------|------------|------------|------------|------------|
| 0     | 0     | SAS        | SAS        | SAS        | SAS        |
| 0     | 1     | SAS        | SAS        | SATA       | SATA       |
| 1     | 0     | SATA       | SATA       | SAS        | SAS        |
| 1     | 1     | SATA       | SATA       | SATA       | SATA       |

**Input Equalization (EQ0A, EQ1A, EQ0B, EQ1B)**

The MAX14980 features control logic inputs (EQ0A, EQ1A, EQ0B, EQ1B) to enable input equalization on each channel, providing 3dB of boost (see Note 4 in the *Electrical Characteristics* table). Drive EQ\_ high to enable input equalization. Drive EQ\_ low to disable input equalization (see Table 3). EQ0A, EQ1A, EQ0B, and EQ1B have internal pulldown resistors of 70k $\Omega$  (typ).

**Output Preemphasis (PE0A, PE1A, PE0B, PE1B)**

The MAX14980 features control logic inputs (PE0A, PE1A, PE0B, PE1B) to enable output preemphasis on either channel, providing 3dB of boost. The MAX14980 true preemphasis, the transition signal, is increased after a changing bit, thus increasing the total energy content of the signal when employed. Drive PE\_ high to enable output preemphasis. Drive PE\_ low to disable output preemphasis (see Table 4). PE0A, PE1A, PE0B, and PE1B have internal pulldown resistors of 70k $\Omega$  (typ).

**Table 3. Input Equalization (EQ0\_, EQ1\_)**

| EQ1_ | EQ0_ | CHANNEL 1_<br>(dB) | CHANNEL 0_<br>(dB) |
|------|------|--------------------|--------------------|
| 0    | 0    | 0                  | 0                  |
| 0    | 1    | 0                  | 3 (typ)            |
| 1    | 0    | 3 (typ)            | 0                  |
| 1    | 1    | 3 (typ)            | 3 (typ)            |

**Table 4. Output Preemphasis (PE0\_, PE1\_)**

| PE1_ | PE0_ | CHANNEL 1_<br>(dB) | CHANNEL 0_<br>(dB) |
|------|------|--------------------|--------------------|
| 0    | 0    | 0                  | 0                  |
| 0    | 1    | 0                  | 3 (typ)            |
| 1    | 0    | 3 (typ)            | 0                  |
| 1    | 1    | 3 (typ)            | 3 (typ)            |

**Applications Information****Exposed Pad Package**

The exposed pad, 42-pin TQFN package incorporates features that provide a very low thermal resistance path for heat removal from the IC. The exposed pad on the MAX14980 must be soldered to GND for proper thermal and electrical performance. For more information on exposed paddle packages, refer to Maxim Application Note HFAN-08.1: *Thermal Considerations of QFN and Other Exposed-Paddle Packages*.

**Layout**

Use controlled-impedance transmission lines to interface with high-speed inputs and outputs of the MAX14980. Place 2.2 $\mu$ F and 0.01 $\mu$ F power-supply bypass capacitors as close as possible to V<sub>CC</sub>, recommended on each V<sub>CC</sub> pin.

**Power-Supply Sequencing**

**Caution:** Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the device.

Proper power-supply sequencing is recommended for all devices. Always apply V<sub>CC</sub> before applying signals, especially if the signal is not current limited.

**Ordering Information**

| PART         | PIN-PACKAGE | TEMP RANGE     |
|--------------|-------------|----------------|
| MAX14980ETO+ | 42 TQFN-EP* | -40°C to +85°C |

+Denotes a lead(Pb)-free/RoHS-compliant package.

\*EP = Exposed pad.

**Chip Information**

PROCESS: BiCMOS

**Package Information**

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO.             | LAND PATTERN NO.        |
|--------------|--------------|-------------------------|-------------------------|
| 42 TQFN-EP   | T423590M+1   | <a href="#">21-0181</a> | <a href="#">90-0079</a> |

MAX14980

## Ruggedized Quad SAS/SATA Redriver/Equalizer with Extended Operating Temperature

### Revision History

| REVISION<br>NUMBER | REVISION<br>DATE | DESCRIPTION     | PAGES<br>CHANGED |
|--------------------|------------------|-----------------|------------------|
| 0                  | 3/13             | Initial release | —                |

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at [www.maximintegrated.com](http://www.maximintegrated.com).

*Maxim Integrated cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim Integrated product. No circuit patent licenses are implied. Maxim Integrated reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the Electrical Characteristics table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.*



Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



#### Как с нами связаться

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